REMARKS

Applicants thank the Examiner for total consideration given the present application. Claims 1 and 4-12 are currently pending of which claims 1, 4, 9, 11, and 12 are independent. Claims 1, 4, 6, 8, 11, and 12 have been amended through this Reply. Upon careful review, one would conclude that no new matter has been added to the application via this amendment. Applicants respectfully request reconsideration of the rejected claims in light of the amendment and remarks presented herein, and earnestly seek timely allowance of all pending claims.

ALLOWABLE SUBJECT MATTER

Applicants appreciate that claim 11 would be allowable if rewritten or amended to overcome the outstanding rejection under 35 U.S.C. § 112, second paragraph.

CLAIM REJECTION UNDER 35 U.S.C. § 112, SECOND PARAGRAPH

The Examiner has rejected claim 11 under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite because there is insufficient antecedent basis for the limitation "said SPST". Although Applicants do not necessarily agree with the Examiner that claim 11 is indefinite, this claim has been amended through this Reply by removing SPST and inserting MPMT therein in order to expedite prosecution. Accordingly, Applicants respectfully request withdrawal of this rejection.

CLAIM REJECTIONS UNDER 35 U.S.C. § 102(b)

Claims 1 and 9 stand rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by Nakahara et al. (U.S. Patent No. 5,485,130)[hereinafter "Nakahara"].

Claims 1 and 9 stand further rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by Matsunaga et al. (U.S. Patent No. 4,789,846)[hereinafter "Matsunaga"].

Claim 12 is rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by Wallace (U.S. Patent No. 6,137,377)[hereinafter "Wallace"].

These rejections are respectfully traversed.

For a Section 102 rejection to be proper, the cited reference must teach or suggest each and every claimed element. *See M.P.E.P. 2131; M.P.E.P. 706.02.* Thus, if the cited reference fails to teach or suggest one or more elements, then the rejection is improper and must be withdrawn.

Nakahara Fails to Anticipate Independent Claims 1 and 9

In this instance, it is respectfully submitted that Nakahara fails to teach or suggest each and every claimed element. For example, independent claims 1 and 9 recite, *inter alia*, "a plurality of field-effect transistor (FET) switches, ***each of said plurality of FET switches is connected in parallel with each other***." *Emphasis added.*

It is respectfully submitted that Nakahara fails to teach or suggest the above-identified claim feature.

As previously submitted, Nakahara discloses a number of different switch circuits. For example, Figure 1 discloses a SPDT switch, however, the field-effect transistors are ***neither connected in parallel with each other*** nor connected directly between the input terminal of the SPST switch and the output terminal of the SPST switch. Figure 7 discloses a switch in which two field-effect transistors separated by a transmission line (14). Therefore, Figure 7 ***fails to disclose*** a plurality of field-effect transistor (FET) switches, each of which is ***connected in parallel with each other***. In addition, Figure 7 fails to disclose field-effect transistors in which the inputs of the field-effect transistors are connected directly between the input terminal of the SPST switch and the output terminal of the SPST switch.

Therefore, for at least these reasons, independent claims 1 and 9 are distinguishable from Nakahara.

Accordingly, Applicant respectfully requests that the rejection of claims 1 and 9, based on Nakahara, be withdrawn.

Matsunaga Fails to Anticipate Independent Claims 1 and 9

In this instance, it is respectfully submitted that Matsunaga fails to teach or suggest each and every claimed element. For example, independent claims 1 and 9 recite, *inter alia*, "a

plurality of field-effect transistor (FET) switches, ***each of said plurality of FET switches is connected in parallel with each other***." *Emphasis added.*

It is respectfully submitted that Matsunaga fails to teach or suggest the above-identified claim feature.

As previously submitted, Matsunaga discloses a number of different semiconductor switches. For example, Figure 6 discloses a SPDT switch, however, the field-effect transistors are ***neither connected in parallel with each other*** nor connected directly between the input terminal of the SPST switch and the output terminal of the SPST switch. Figures 5(a), 5(b) and 6 disclose FET 14 and FET 38 which are *not directly* connected in parallel, rather, there is a one quarter wave length between drain 15 of FET 14 and drain 40 of FET 14 (Column 7, lines 46 to 56). Therefore, Matsunaga fails to disclose a plurality of field-effect transistor (FET) switches, each of which is ***connected in parallel with each other***. In addition, Matsunaga fails to disclose field-effect transistors connected directly between the input terminal of the SPST switch and the output terminal of the SPST switch.

Therefore, for at least these reasons, independent claims 1 and 9 are distinguishable from Matsunaga.

Accordingly, Applicant respectfully requests that the rejection of claims 1 and 9, based on Matsunaga, be withdrawn.

Wallace Fails to Anticipate Claim 12

In this instance, it is respectfully submitted that Wallace fails to teach or suggest each and every claimed element. For example, amended independent claim 12 recites, *inter alia*, "***wherein said FET switches having their first terminals connected to corresponding input terminal or output terminal of the said MPMT switch and wherein said FET switches having their second terminals connected with each other***." *Emphasis added.*

It is respectfully submitted that Wallace fails to teach or suggest the above-identified claim feature.

Wallace merely discloses a conventional MMIC circuitry which allows reception of electronically selectable single polarity or simultaneous dual polarity/dual beam signals by placed-array modules. Although in Fig. 7C, Wallace illustrates two transistors connected in series for DC biasing, nowhere does Wallace teach or suggest a plurality of FET switches ***having their first terminals connected to corresponding input terminal or output terminal of the a MPMT switch and having their second terminals connected with each other***.

Therefore, for at least these reasons, independent claim 12 is distinguishable from Wallace.

Accordingly, Applicant respectfully requests that the rejection of claim 12, based on Wallace, be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. § 103(A)

Claims 1, 4-8 and 10 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Tokumitsu et al. (JP 05-299995)[hereinafter "Tokumitsu"] in view of Nakahara or Matsunaga. Applicants respectfully traverse this rejection

Applicants respectfully submit that the Examiner has failed to establish a *prima facie* case of obviousness. To establish a *prima facie* case of obviousness, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). Additionally, there must be a reason why one of ordinary skill in the art would modify the reference or combine reference teachings to obtain the invention. A patent composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art. *KSR Int'l Co. v Teleflex Inc.*, 82 USPQ2d 1385 (U.S. 2007). There must be a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does. *Id.* The Supreme Court of the United States has recently held that the "teaching, suggestion, motivation test" is a valid test for obviousness, albeit one which cannot be too rigidly applied. *Id.* Rejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational

underpinning to support the legal conclusion of obviousness. *Id.*

In this instance, it is respectfully submitted that the combination of Tokumitsu and Nakahara or Matsunaga fails to render independent claims 1 and 4 obvious.

For example, independent claim 1 now recites, *inter alia*, "a plurality of field-effect transistor (FET) switches, ***each of said plurality of FET switches is connected in parallel with each other***." (*Emphasis added.*)

As previously submitted, Figure 6 of Tokumitsu discloses a SPDT switch. The SPDT switch of Tokumitsu has a parallel circuit in series with a capacitor, the parallel circuit being a gate in parallel with an inductor. Additionally, the parallel circuit in series with a capacitor is a first portion of a switch, which is in parallel with a second portion of a switch consisting of a gate in series with an inductor. Thus, Tokumitsu fails to disclose a SPST switch comprising "a plurality of field-effect transistor (FET) switches, ***each of said plurality of FET switches is connected in parallel with each other***."

As demonstrated above in great detail, neither Nakahara nor Matsunaga teaches or suggests the above-identified feature of claim 1. Thus, it is respectfully submitted that the combination of Tokumitsu and Nakahara or Matsunaga fails to render independent claim 1 obvious.

Independent claim 4 now recites, *inter alia*, "a field-effect transistor (FET) switch constructed by directly connecting an inductor in parallel with a series circuit, the series circuit consisting of a capacitor connected in series with a drain or source of FET, wherein ***if the drain of the FET is directly connected with the capacitor, then the source of the FET is connected with the input terminal of said SPST switch and if the source of the FET is directly connected with the capacitor, then the drain of the FET is connected with the input terminal of said SPST switch*** . . . said ***FET has a parasitic inductor and said capacitor causing series resonance with parasitic inductance of the FET, and the inductor causing parallel resonance with parasitic capacitance of the FET and the capacitor***." (*Emphasis added.*)

As previously submitted, Tokumitsu describes a microwave semiconductor switch that consists of two circuit portions in parallel with each other (Abstract and Figure 1). The first

circuit portion consists of a switch in series with an inductor. The second circuit portion consists of a parallel circuit in series with a capacitor, the parallel circuit being a field-effect transistor in parallel with an indictor (Abstract and Figure 1).

It is respectfully submitted that nowhere does Tokumitsu teach or suggest a field-effect transistor (FET) switch constructed by directly connecting an inductor in parallel with a series circuit, the series circuit consisting of a capacitor connected in series with a drain or source of FET, wherein if the drain of the FET is directly connected with the capacitor, then the source of the FET is connected with the input terminal of said SPST switch and if the source of the FET is directly connected with the capacitor, then the drain of the FET is connected with the input terminal of said SPST switch.

In addition, it is respectfully submitted that nowhere does Tokumitsu teach or suggest that the FET has a parasitic inductor and the capacitor causing series resonance with parasitic inductance of the FET, and the inductor causing parallel resonance with parasitic capacitance of the FET and the capacitor.

Further, it is respectfully submitted that neither Nakahara nor Matsunaga fulfills the above-noted deficiency of Tokumitsu with respect to the amended feature of claim 4.

At least in view of the above, Applicants respectfully submit that the asserted combination of Tokumitsu and Nakahara or Matsunaga (assuming these references may be combined, which Applicants do not admit) fails to establish *prima facie* obviousness of claims 1 and 4 or any claim depending therefrom. Accordingly, reconsideration and withdrawal of this rejection is respectfully requested.

CONCLUSION

In view of the above amendment, Applicants believe the pending application is in condition for allowance.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Ali M. Imam Reg. No. 58,755 at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37.C.F.R. §§1.16 or 1.17; particularly, extension of time fees.

Dated: August 27, 2009

Respectfully submitted,

By #58,755

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